said time-keeping clock signal generation circuit in response to time-keeping by said time-keeping clock signal generation circuit.

9. An electronic apparatus according to Claim 7, wherein said electronic apparatus comprises a camera.

10. (Amended) An electronic apparatus according to Claim 7, further comprising a control circuit that controls said electronic apparatus, and wherein said control circuit includes a central processing unit.

REMARKS

Claims 1 through 10 are presented for examination. Claims 1 and 7 are the independent claims. Claims 1 to 3 and 6 to 8 have been amended.

In the Official Action, the drawings were objected to on formal grounds, and Claims 7 to 10 were rejected under 35 U.S.C. § 112, first and second paragraphs, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, and as indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1 and 4 were rejected under 35 U.S.C. § 102(b), as anticipated by U.S. Patent No. 5,854,950 (Handa); Claims 2, 7 and 9 were rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa '950 patent in view of U.S. Patent No. 6,285,625 (Vogley); Claims 3 and 5 were rejected under 35

U.S.C. § 103(a), as unpatentable over the Handa '950 patent in view of U.S. Patent No. 4,825,233 (Kanai); Claim 6 was rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa '950 patent in view of Japanese Laid-Open Patent No. 06-250278 (Kitani); and Claims 8 and 10 were rejected under 35 U.S.C. § 103(a), as unpatentable over the Handa '950 patent in view of the Vogley '625 patent, further in view of the Kanai '233 patent. Reconsideration and withdrawal of the objection and the rejections respectfully are requested in view of the above amendments and the following remarks.

The formal rejections of Claims 7 to 10 respectfully are traversed. Nevertheless, without conceding the propriety of the rejections, Claims 7 and 8 further have been amended herein even more clearly to conform the claim language with the features illustrated in the drawings (see Figure 1) and described in the written disclosure; Applicant submits that those skilled in the art readily will understand the recited features of "a time-keeping clock signal generation circuit" and "a ferroelectric memory time-keeping counter circuit", as disclosed and claimed in the present application. In this regard, Applicant notes that each of these features relates to a *circuit* (i.e., a ferroelectric memory circuit), not simply an element (i.e., a ferroelecttric memory). Reconsideration and withdrawal of the formal rejections respectfully are requested.

The objection to the drawings respectfully is traversed for the same reasons. As noted above, the claim language has been amended to find clear antecedent basis in the drawings and the corresponding written disclosure. Reconsideration and withdrawal of the objection respectfully are requested.

The present invention relates to a novel electronic apparatus. In one aspect, as now recited in Independent Claim 1, the present invention relates to an electronic apparatus comprising a clock circuit that generates a clock signal having clock signal pulses generated at a predetermined cycle, and a non-volatile memory time-keeping counter circuit for counting clock signal pulses generated by the clock circuit and storing a count of the clock signal pulses. That is, in the electronic apparatus, a clock circuit generates a clock signal having clock signal pulses generated at a predetermined cycle, and a non-volatile memory circuit counts the clock signal pulses generated by the clock circuit and stores a count of the clock signal pulses.

In another aspect, as now recited in independent Claim 7 the present invention relates to an electronic apparatus comprising a time-keeping clock signal generation circuit that keeps time, and a ferroelectric memory time-keeping counter circuit that forms and stores a time signal concerning time kept by the time-keeping circuit.

Applicant submits that the prior art fails to anticipate the present invention. Moreover, Applicant submits that there are differences between the subject matter sought to be patented and the prior art, such that the subject matter taken as a whole would not have been obvious to one of ordinary skill in the art at the time the invention was made.

The Handa '950 patent relates to a data recording device for a camera and film type camera with lens, and. discloses a data recording device capable of preventing the recording of incorrect date and time data on photographic film due to malfunction of the time counter that generates date and time data for recording. A drive of the data recording device has a time counter that generates date and time data for recording. The count value of the date and time data generated by this time counter are stored in a storage circuit. However, Applicant submits

that the Handa '950 patent fails to disclose or suggest at least the above-described features of the present invention. In particular, Applicant understands the Handa '950 patent arrangement to require that the clock pulses be counted in a time counter 161 and that the count value of the time counter be stored in a storage circuit 33 separate from the time counter. Further, immediately prior to the operation that changes the count value of the time counter, the date and time data in the storage circuit and the counter value of the date and time data from the time counter are compared in a comparison judgment circuit. If the two do not agree, a malfunction detection signal which indicates that the time counter has malfunctioned is output to the driver and the recording of date and time data by liquid crystal display panel is stopped.

The Vogley '625 patent relates to a high speed clock circuit for a semiconductor memory device, and discloses a synchronous dynamic random access memory that operates in synchronism with differential clock signals (CLK and /CLK). A timing and control circuit compares the complementary differential clock signals (CLK and /CLK) to generate an internal clock signal (CLKI) so as to compensate for degradations in the differential clock signals (CLK and /CLK). Utilizing the internal timing signal (CLKI) avoids employing more complex circuits that must operate in synchronism with the edges of both differential clock signals (CLK and /CLK). However, Applicant submits that the Vogley /625 patent fails to disclose or suggest at least the above-described features of the present invention. In paricular, Applicant submits that the Vogley /625 patent fails to disclose that an EEPROM and a ferroelectric memory are interchangeable, as suggested by the Examiner. Rather, the Vogley '625 patent is understood merely to discloses a clocking arrangement for a random access memory in which complementary differential clock signals are compared to generate a single internal timing signal

for clocking the memory, and further that both a ferroelectric memory and an EEPROM may both benefit from this clock timing arrangement. Nor is the Vogley '625 patent understood to add anything to the Handa '950 patent that would make obvious the claimed invention.

The Kanai '233 patent relates to a data recording camera, and was cited for its teaching of a camera having a clock circuit and a corresponding memory circuit. However, Applicant submits that the Kanai /233 patent fails to disclose or suggest at least the above-discussed features of the present invention. Nor is the Kanai '233 patent understood to add anything to the Handa '950 patent and/orthe Vogley '625 patent that would make obvious the claimed invention.

The JP '278 reference relates to camera apparatus, and was cited for its teaching of a nonvolatile memory circuit that starts counting a state in which a predetermined value is added to the memory contents of the nonvolatile memory circuit when a power supply (power cell 43) for supplying power to the camera is replaced for eliminating the need for a backup supply voltage. However, Applicant submits that the JP '278 reference fails to disclose or suggest at least the above-discussed features of the present invention. Nor is the JP '278 reference understood to add anything to the Handa '950 patent, the Vogley '625 patent and/or the Kanai '233 patent that would make obvious the claimed invention.

A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

For the above reasons, Applicant submits that Claims 1 and 7 are allowable over the cited art.

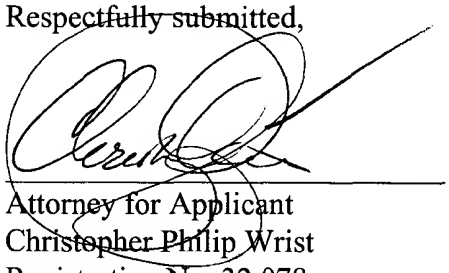
Claims 2 to 6 and 8 to 10 depend from Claims 1 and 7, respectively, and are believed allowable for the same reasons. Moreover, each of these dependent claims recites additional features in combination with the features of its respective base claim, and is believed allowable in its own right. Individual consideration of the dependent claims respectfully is requested.

Applicant requests that the present Amendment be entered under 37 CFR 1.116. Applicant submit that the proposed amendments merely are formal or minor in nature, do not add any significant new issues for consideration, and place the application in condition for allowance. Applicant submits that the present amendments were necessitated by the Examiner's comments in the Official Action and were not previously made because Applicant believes the prior claims are allowable.

Applicant submits that the present Amendment is fully responsive to each of the points raised by the Examiner in the Official Action, and that the Application is in condition for allowance. Favorable consideration of the claims, and passage to issue of the application at the Examiner's earliest convenience earnestly are solicited.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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MARKED-UP VERSION SHOWING CHANGES TO THE CLAIMS

1. (Twice Amended) An electronic apparatus comprising:

a clock circuit that generates a clock signal having clock signal pulses generated at a predetermined cycle; and

a non-volatile memory time-keeping counter circuit for counting clock signal pulses generated by said clock circuit and storing a count of the clock signal pulses.

2. (Amended) An electronic apparatus according to Claim 1, wherein said non-volatile memory time-keeping counter circuit comprises a ferroelectric memory.

3. (Amended) An electronic apparatus according to Claim 1, further comprising:

a control circuit that controls said electronic apparatus,

wherein said control circuit controls said non-volatile memory time-keeping counter circuit so as to count the clock signal pulses in response to the clock signal generated by said clock signal circuit.

6. (Amended) An electronic apparatus according to Claim 1, wherein, when a power supply battery for supplying power to said electronic apparatus is replaced, said non-volatile memory time-keeping counter circuit starts counting in a state in which a predetermined value is added to the memory contents of said non-volatile memory time-keeping counter circuit.

7. (Twice Amended) An electronic apparatus comprising:

a time-keeping clock signal generation circuit that keeps time: and

a ferroelectric memory time-keeping counter circuit that forms and stores a time signal concerning time kept by said time-keeping circuit.

8. (Amended) An electronic apparatus according to Claim 7, further comprising a control circuit that controls the electronic apparatus, wherein said control circuit controls said ferroelectric memory time-keeping counter circuit so as to store the time signal for said time-keeping clock signal generation circuit in response to time-keeping by said time-keeping clock signal generation circuit.